MULTIMEDIA UNIVERSITY

STUDENT ID NO

Table NO	

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2, 2016/2017

PDS0101 – INTRODUCTION TO DIGITAL SYSTEMS

(All sections / Groups)

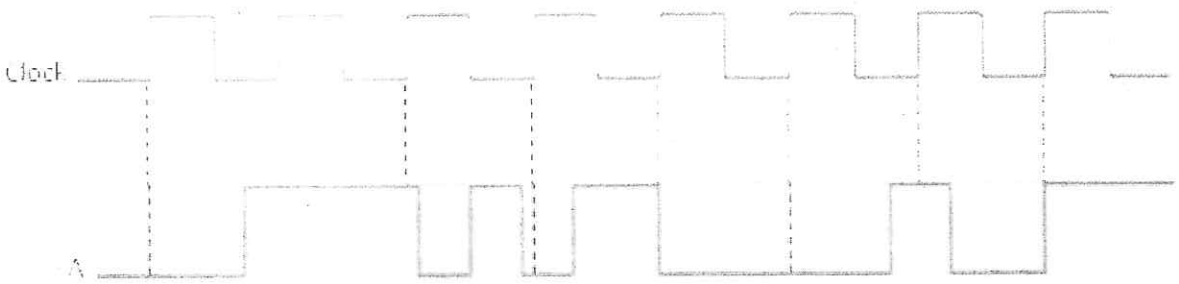
24 February 2017
3.00 pm - 5.00 pm
(2 Hours)

INSTRUCTIONS TO STUDENTS

1. This Question paper consists of 10 pages including cover page with 5 Questions. Please attempt **ALL** questions.
2. The total marks for this paper is 50 marks and the distribution of the marks for each question is given.
3. Please print all your answers in this booklet.

QUESTION 1

a) Referring to the square waveform T shown in the image below, answer the questions that follow.



i. Determine whether the waveform is periodic or non-periodic. State your reason.
ii. Indicate the sequence of bits transferred if a bit is read upon the clock's rising edge.
iii. What is the time required to send one (1) bit if given the reference clock is running at 80 Hz?
iv. Calculate the total time required to send the bits you determined in (ii) for 8 bit parallel bus transfer.

[4 Marks]

b) Convert the following:

i. 1001.111_2.....Binary number to decimal
ii. 4573_8 ..... Octal to decimal
iii. 55.625_{10}.....Decimal to binary

[3 Marks]

Continued ...

c) Perform the calculation of $27_{10} - 39_{10}$ using 8-bits signed 2's complement binary numbers and provide your answer in decimal.

[3 Marks]

QUESTION 2

a) Prove that $AB\overline{C} + B\overline{C}D + \overline{A}(B\overline{C} + A) = B\overline{C}$ by using Boolean algebra rules. **[3 Marks]**

Continued ...

b) It is given that $W = \left(AB + \overline{C}\right)(B + \overline{A})$. Find the output of W by completing the truth table.

[3 Marks]

A	B	C	AB	$\overline{C}$	$AB + \overline{C}$	$\overline{A}$	$B + \overline{A}$	$W = \left(AB + \overline{C}\right)(B + \overline{A})$
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

c) By applying Boolean rules and theorems, simplify the given expression K, and then draw the logic circuit for the simplified K.

[2+2 = 4 Marks]

$$K = (W + \overline{X})(Y + \overline{W}) + \overline{XY}$$

Continued ...

QUESTION 3

a) Derive the Boolean expression of M in standard Sum of Products (SOP) format for the given truth table. **[3 Marks]**

Input			Output
A	B	C	M
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

b) Apply K-map to minimize the Boolean expression in SOP form and draw the simplified circuit.

[3 Marks]

Continued ...

c) Construct a truth table for the Boolean expression P. By applying Boolean rules and theorems, simplify the given expression P.

$$P = \overline{\overline{X}\overline{Y}} + \overline{X\overline{Y}}$$

[4 Marks]

QUESTION 4

a) Design a 4-bit parallel adder by using four full adders, where carry output is represented by C_1, C_2, C_3, C_4 and sum of each bit adder is represented by $\sum_1$, $\sum_2$, $\sum_3$ and $\sum_4$.

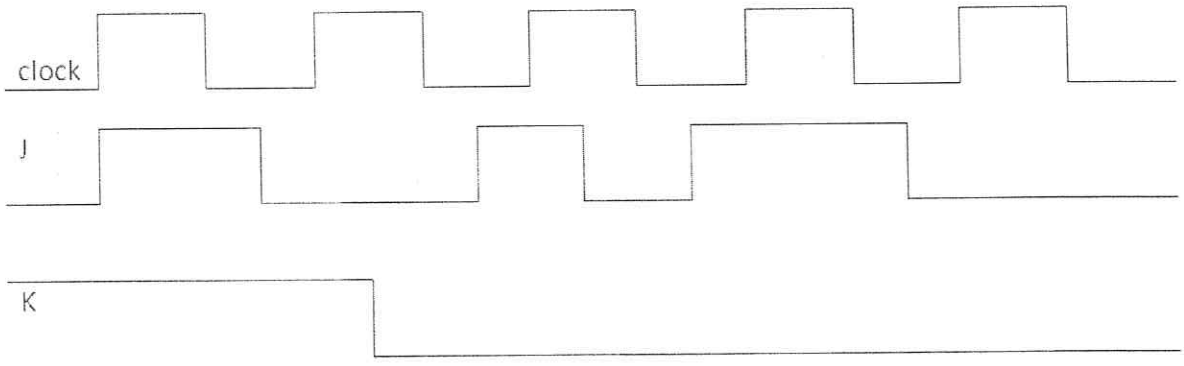
[3 marks]

Continued ...

b) By referring to the 4-bit parallel adder in (a), what is the result for C_1, C_2, C_3, C_4 and sum of each bit adder $\sum_1$, $\sum_2$, $\sum_3$, $\sum_4$ when 0101_2 and 1111_2 are added together.

[4 marks]

c) For a positive edge triggered (PGT) J-K flip-flop with inputs as shown below, determine the Q (normal) output relative to the CLK assuming that Q is initially LOW. **[3 Marks]**



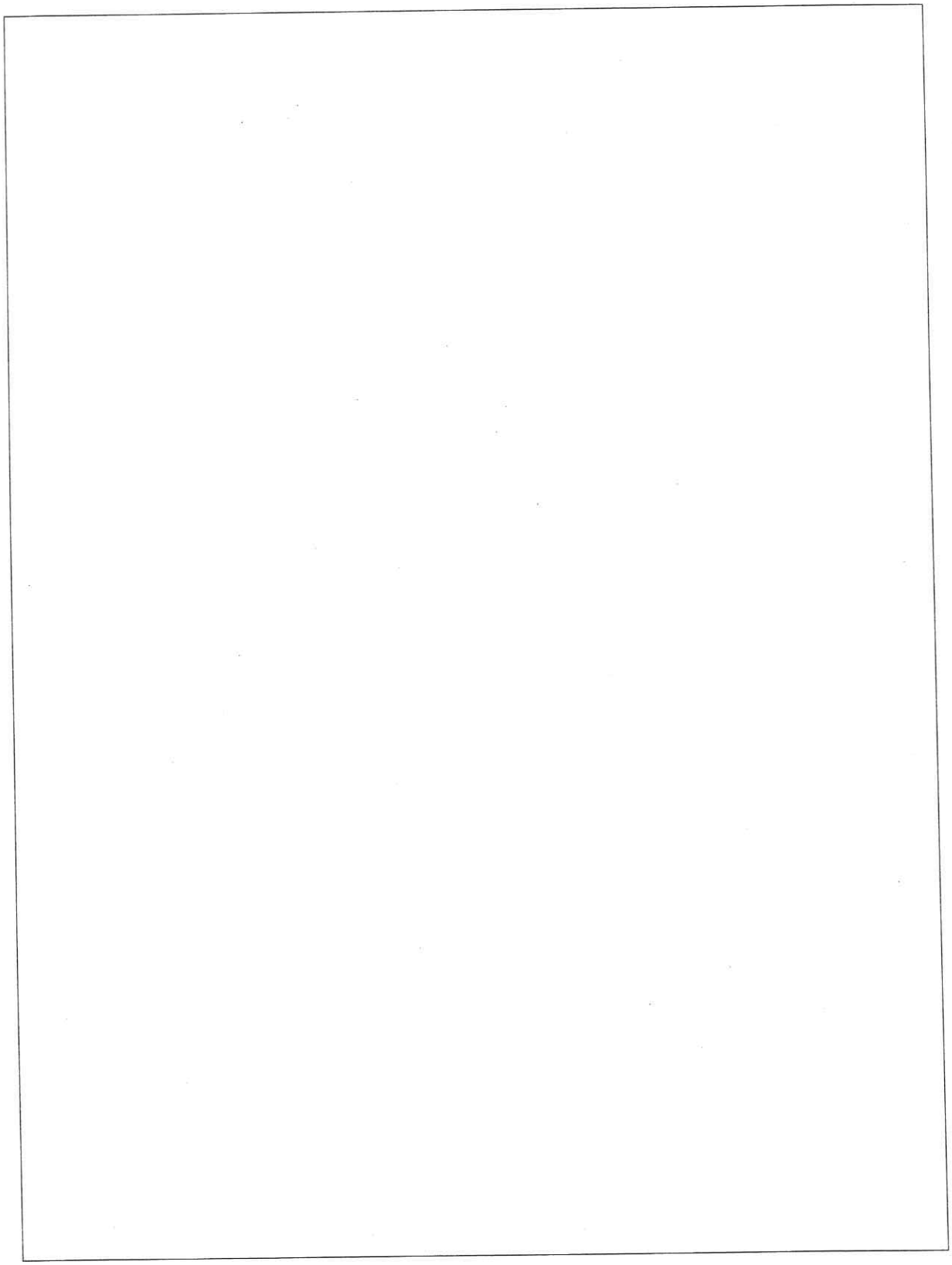
Continued ...

QUESTION 5

Design a synchronous counter using JK flip-flops that follows the sequence 100,101,010,001 and repeats. The undesired states go to 001 on the next clock pulse.

a) Construct the state diagram for the counter. **[2 Marks]**
b) Create the next state table according to the state diagram in (a) **[2 Marks]**
c) Use J-K excitation table to define the J and K inputs for each flip-flop involved in the counter. **[2 Marks]**
d) Perform K-map simplification for each of the flip-flops in the counter. **[2 Marks]**
e) Implement the simplified expressions as combinational logic using JK flip-flops to complete the design of the counter. **[2 Marks]**

Continued ...



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End of Exam